LISTING OF THE CLAIMS:

This listing of the claims replaces all prior versions, and listings, of claims in the application. Please amend the claims as follows:

1. (Currently Amended) In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of simulation processors having a plurality of outputs;

a first reconfigurable interconnect stage ~~configurable~~ having a plurality of inputs ~~to receive~~ coupled to the outputs from the simulation processors, and further having a plurality of outputs;

a second reconfigurable interconnect stage having a plurality of inputs ~~configurable to receive~~ coupled to a first subset of the outputs from the first reconfigurable interconnect stage, and further having a plurality of outputs, wherein a first subset of the outputs from the second reconfigurable interconnect stage are coupled to a first subset of the inputs of the first reconfigurable interconnect stage via a plurality of feedback paths; and

a third reconfigurable interconnect stage having a plurality of inputs ~~configurable to receive~~ coupled to a second subset of the outputs from the second reconfigurable interconnect stage~~, and further configurable to provide outputs to inputs of the second reconfigurable interconnect stage~~,

wherein the plurality of feedback paths each couples one of the outputs of the second reconfigurable interconnect stage to one of the inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage.

2. (Currently Amended) The reconfigurable interconnect network of claim 1, wherein a second subset of the outputs from the ~~second~~ first reconfigurable interconnect stage ~~is further configurable to provide outputs~~are coupled to inputs of the simulation processors.

3. (Currently Amended) The reconfigurable interconnect network of claim 1, further including a memory coupled to the first, second, and third reconfigurable interconnect ~~stage~~stages,

each of the ~~second~~ first, second, and third reconfigurable interconnect ~~stage~~ stages being dynamically configured in accordance with a content of the memory.

4. (Currently Amended) In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of clusters, each cluster including:

a plurality of simulation processors, and

a first reconfigurable interconnect stage configurable to receive outputs from the simulation processors in the cluster;

a second reconfigurable interconnect stage configurable to receive a first plurality of outputs from the first reconfigurable interconnect stages and to provide a first plurality of outputs back to inputs of the first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage configurable to receive a second plurality of outputs of the second reconfigurable interconnect stage and to provide outputs back to inputs of the second reconfigurable interconnect stage,

wherein the first plurality of outputs of the second reconfigurable interconnect stage is each coupled to one of the inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage.

5. (Currently Amended) The reconfigurable interconnect network of claim 4, wherein the ~~second~~ first reconfigurable interconnect stage is further configurable to provide a second plurality of outputs back to inputs of the simulation engines of the clusters.

6. (Currently Amended) In a logic simulation system, a reconfigurable interconnect network comprising:

a first reconfigurable interconnect stage;

a second reconfigurable interconnect stage configurable to receive outputs from the first reconfigurable interconnect stage and to provide a first plurality of outputs back to inputs of the

first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage configurable to receive a second plurality of outputs from the second reconfigurable interconnect stage and provide outputs back to the second reconfigurable interconnect stage,

wherein the first plurality of outputs of the second reconfigurable interconnect stage is each coupled to one of the inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage.

7. (Original) The reconfigurable interconnect network of claim 6, wherein the first reconfigurable interconnect stage is coupled to outputs from a plurality of simulation processors.

8. (Currently Amended) In a logic simulation system, a reconfigurable interconnect network comprising:

a plurality of simulation processors;

a first reconfigurable interconnect stage having a first plurality of inputs coupled to outputs of the simulation processors;

a second reconfigurable interconnect stage having a first plurality of inputs coupled to outputs of the first reconfigurable interconnect stage and a first plurality of outputs coupled to a second plurality of inputs of the first reconfigurable interconnect stage; and

a third reconfigurable interconnect stage having inputs coupled to a second plurality of outputs of the second reconfigurable interconnect stage, and further having outputs coupled to a second plurality of inputs of the second reconfigurable interconnect stage,

wherein the first plurality of outputs of the second reconfigurable interconnect stage is each coupled to one of a second plurality of inputs of the first reconfigurable interconnect stage without passing through the third reconfigurable interconnect stage.

9. (Currently Amended) The reconfigurable interconnect network of claim 8, wherein the second plurality of outputs of the second reconfigurable interconnect stage are coupled to the

inputs of the third reconfigurable interconnect stage using a butterfly topology.

10. (Currently Amended) The reconfigurable interconnect network of claim 8, wherein the second and third reconfigurable interconnect stages ~~are~~ each comprises a plurality of crossbars.

Claims 11-14. (Canceled).